COURSE STAFF

Course Lecturer: Dr. Aron Michael, Room EE 241
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Consultations: Consultation times through the week will be agreed upon with students in the first couple of weeks of lectures to arrive at times that suit most students. Apart from these consultation times, students may send e-mail to arrange other consultation times. Students are strongly encouraged to use the agreed upon consultation times to discuss any technical and other issues in the course.

COURSE DETAILS

Credits:
The course is a 6 UoC course; expected workload is about 10 hours per week throughout the 12 week session.

Contact hours:
The course consists of 3 hours of lectures per week, and laboratory demonstrations will be given during lectures time when needed.

Lectures:
Thursdays, 6pm-9pm (REDC M0101)

Computer Labs:
Room EEG19

COURSE INFORMATION

Scopes:
This is a postgraduate course. The main focus of the subject is on semiconductor processes involved in the fabrication of very large scale silicon integrated circuits. Initially, the course will attempt to study individual processes, and towards the end these processes are integrated together into a process schedule for the fabrication of CMOS and bipolar VLSI circuits. Because integrated circuits fail from time to time, failure analysis plays an important role in process development. The course will include lectures on analytical techniques employed in understanding the causes of failure in order to modify the processes for better reliability.

VLSI technology is moving at a very rapid pace, spurred by the demand for further and further miniaturisation, greater circuit complexity and functionality per chip. Minimum feature sizes in production in ‘60s were tens of µm. In the ‘70s, it was several µm, in the ‘80s it was about 1µm, in the ‘90s it is submicron and now in the 21st century, it is the deep-deep-sub micron (<50nm range). Acronyms have evolved from SSI to MSI to LSI to VLSI to ULSI to GSI and now Terascale a head are enormous. In the past 20 years, ‘ultimate’ limits of scaling were predicted, and only to be surpassed years later. Wafer size of 300mm is now in production and will move to 450mm by 2012!!

The subject will enable students to have a broad grasp of the multi-disciplinary nature of the VLSI technology, bringing together the know-how of physicist, chemist, engineers and mathematicians. It will provide the basics for students, who may enter the semiconductor industry, to build on. It is an exciting field of research and we should count ourselves fortunate to be witnessing and participating in this era of unparalleled ‘technology explosion’.

**Aims:**
The course aims to familiarize students with silicon integrated technology and equip them with fundamental know-hows on which they build their future career in the semiconductor fabrication foundries and research areas.

**Relation to other courses:**
This is a postgraduate course offered to students in the Master of Engineering Science at the University of New South Wales. The course complements the microelectronics design courses ELEC4602 and ELEC 9701. It lays the ground work for Microsystems Course ELEC 9703.

**Pre-requisites:**
There is no specific pre-requisite for the course. However, it suits to students who are familiar with semiconductor device and microelectronics design similar to the course covered in ELEC4603 and ELEC4602 in EE undergraduate program.
Assumed Knowledge:

It is further assumed that the students are familiar with some basic chemistry. The course is multidisciplinary in nature.

Following Courses:

The course lays the ground work for Microsystems design and technology, ELEC9703.

References:

The textbook set for this course is:

Additionally, the following books are good additional resources for topics in the course:

Learning outcomes and attributes:

After the successful completion of the course, the student will be able to:

1. Understand the basic process steps in making integrated circuits
2. Understand how these steps are integrated in the process
3. Understand the technology limitations of each process
4. Understand the impact of these limitations on the IC designer’s options
5. Develop an appreciation of the technology trends

Contribution of course to graduate attributes:

The course delivery methods and course content address a number of core UNSW graduate attributes; these include:
1. The capacity for analytical and critical thinking and for creative problem-solving, which is addressed by the design task and tutorial exercises.
2. The ability to engage in independent and reflective learning, which is addressed by the lectures, assignments, tutorials and laboratory work.
3. The skills of effective communication, which are addressed by reports and oral presentations.
4. Information literacy, which is addressed by the homework.
Please refer to http://www.ltu.unsw.edu.au/content/userDocs/GradAttrEng.pdf for more information about graduate attributes.

**TEACHING STRATEGIES**

**Delivery mode:**
The course consists of the following elements: face-to-face lectures delivered in class and take-home assignment work. The course also uses moodle to post assignments, and their solutions. Other announcements during the length of the courses will also be posted on moodle. Moodle is available at http://moodle.telt.unsw.edu.au.

**Course Schedule:**

<table>
<thead>
<tr>
<th>Week</th>
<th>Major Topics</th>
<th>Lecturer</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1(07/03)</td>
<td>Introduction VLSI technology: Review of VLSI “technology explosion” – a historical perspective, trends, and challenges</td>
<td>AM</td>
<td></td>
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<tr>
<td>2(14/03)</td>
<td>Silicon crystal growth and wafer preparation</td>
<td>AM</td>
<td></td>
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<tr>
<td>3(21/03)</td>
<td>Oxidation of silicon</td>
<td>AM</td>
<td>Quiz -1</td>
</tr>
<tr>
<td>4(28/03)</td>
<td>Impurity diffusion in silicon</td>
<td>AM</td>
<td>Presentation-1</td>
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<td></td>
<td><strong>BREAK</strong></td>
<td></td>
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<tr>
<td>5(11/04)</td>
<td>Ion implantation of impurities into silicon</td>
<td>AM</td>
<td>Quiz-2</td>
</tr>
<tr>
<td>6(18/04)</td>
<td>Epi-taxy growth on silicon substrates</td>
<td>AM</td>
<td>Presentation-2</td>
</tr>
<tr>
<td>7*(25/04)</td>
<td></td>
<td>AM</td>
<td>Public holiday</td>
</tr>
<tr>
<td>8(2/05)</td>
<td>Thin Film deposition techniques</td>
<td>AM</td>
<td>Ass 1 due Quiz-3</td>
</tr>
<tr>
<td>9(9/05)</td>
<td>Etching: wet, Reactive plasma Etching</td>
<td>AM</td>
<td>Ass 2 due Quiz-4</td>
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<tr>
<td>10(16/05)</td>
<td>Lithography, Metallization</td>
<td>AM</td>
<td>Presentation-3</td>
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<tr>
<td>11(23/05)</td>
<td>VLSI process integration, 3D integration</td>
<td>AM</td>
<td>Quiz-5</td>
</tr>
<tr>
<td>12(30/05)</td>
<td>Failure Analysis Techniques</td>
<td>AM</td>
<td>Presentation-4</td>
</tr>
<tr>
<td>13(06/06)</td>
<td>Tutorial</td>
<td>AM</td>
<td>Ass 3 due</td>
</tr>
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Lectures:

The lecture, delivered in class, will cover a range of VLSI technology topics. Beginning with an overall view of the evolution in processing technology from the invention of the transistor until now, topics like silicon crystal growth and wafer preparation, oxidation, diffusion, implantation, epitaxy, thin film deposition, etching, lithography, metallisation, process integration and failure analysis will be covered. Emphasis is on understanding the process and its limitations; see the impact this has on process integration, the IC layout design and circuit performance.

Laboratories:

There is no formal laboratory work in this course. Some out of lecture time will be devoted, where appropriate, to visit the semiconductor Nanofabrication Facility and see demonstration of selected processes. There will be limited exposure to TCAD simulation for some of the processes.

Home work:

The lectures can only cover the course material to a certain depth; students must read the textbook and reflect on its content as preparation for the lectures to fully appreciate the course material. Students are encouraged to read the text book and reference materials. Home preparation before attending lectures will give students maximum benefit.

Self-guided tutorials:

The tutorials/assignments take the student through selected critical course topics, some of which may only be covered superficially, and the aim of the exercise is to make students research on the area themselves. These areas are examinable. The students are strongly encouraged to complete all the tutorial/assignments.

Assignments:

Three major assignments will be set for this course. Assignments will allow the student to explore the subject in greater depth. Deadlines for the submission of assignments are indicated in the course schedule.

Assessment:

There are four components of the assessment in this course:

- **Fortnight quizzes**: 5%
1. **Fortnight quizzes:** 5 mins quiz will be held in class fortnightly just before the lecture. It will start in week 3 and fortnightly from there on. The questions are not meant to be hard and students, who have been following the course, are expected to easily pass, and even score 100%. This is to encourage students to follow the course while rewarding them for doing so.

2. **Assignment:** There are also three compulsory written assignments for this course, which will be released on the course Moodle after Week 2, 6 and 9 respectively. The assignments will each worth 10% of the overall mark in total for this course. It is expected that the students complete assignments on their own. Assignment submissions are set on Wednesdays in week 6, 9, and 13 for each assignment respectively.

3. **Presentation:** there will be group presentations on various topics related to VLSI technology trends, new developments, approaches, and future challenges. The groups can choose other topics provided that they discuss them with the lecturer. The number of students in a group will be decided in week 2 or 3. Presentations will be held for 20min before the lecture in week 4, 6, 10, and 12.

4. **Final exam:** there will be a closed book 3 hour final exam.

Note: For all class assessment tasks, if the student is unable to attend for medical or other serious reasons (e.g. death in the family) the student must present medical certificates and/or other relevant documentations within 3 days of the assessment to the course convener. If this is not done within the required time period, then no consideration will be given. In the case of missing a quiz/test for one of the reasons above, the assessment will be carried over to the final exam, i.e the final exam will become a higher % of the assessment.

**OTHER MATTERS**

Academic honesty and plagiarism:
What is Plagiarism?
Plagiarism is the presentation of the thoughts or work of another as one’s own.* Examples include:
• direct duplication of the thoughts or work of another, including by copying material, ideas or concepts from a book, article, report or other written document (whether published or unpublished), composition, artwork, design, drawing, circuitry, computer program or software, web site, Internet, other electronic resource, or another person’s assignment without appropriate acknowledgement;
• paraphrasing another person’s work with very minor changes keeping the meaning, form and/or progression of ideas of the original;
• piecing together sections of the work of others into a new whole;
• presenting an assessment item as independent work when it has been produced in whole or part in collusion with other people, for example, another student or a tutor; and
• claiming credit for a proportion a work contributed to a group assessment item that is greater than that actually contributed.†

For the purposes of this policy, submitting an assessment item that has already been submitted for academic credit elsewhere may be considered plagiarism.

Knowingly permitting your work to be copied by another student may also be considered to be plagiarism.

Note that an assessment item produced in oral, not written, form, or involving live presentation, may similarly contain plagiarised material.

The inclusion of the thoughts or work of another with attribution appropriate to the academic discipline does not amount to plagiarism.

The Learning Centre website is main repository for resources for staff and students on plagiarism and academic honesty. These resources can be located via:

www.lc.unsw.edu.au/plagiarism

The Learning Centre also provides substantial educational written materials, workshops, and tutorials to aid students, for example, in:

• correct referencing practices;
• paraphrasing, summarising, essay writing, and time management;
• appropriate use of, and attribution for, a range of materials including text, images, formulae and concepts.

Individual assistance is available on request from The Learning Centre.

Students are also reminded that careful time management is an important part of study and one of the identified causes of plagiarism is poor time management.
Students should allow sufficient time for research, drafting, and the proper referencing of sources in preparing all assessment items.

Based on that proposed to the University of Newcastle by the St James Ethics Centre. Used with kind permission from the University of Newcastle

† Adapted with kind permission from the University of Melbourne.

Contact Information:

All queries or concerns about VLSI technology should be directed to a.michael@unsw.edu.au. Please ensure that the subject line of any e-mail sent is informative and includes the word ‘ELEC9704’.

Course improvement:

This course is continually under review and constructive student feedback is always valued. Periodically student evaluative feedback on the course is gathered, using among other means, UNSW's Course and Teaching Evaluation and Improvement (CATEI) Process. Student feedback is taken seriously, and continual improvements are made to the course based in part on such feedback.

Administrative Matters:

It is important that students familiarise themselves with all the School of Electrical Engineering and Telecommunications policy and procedures. These are available at: [http://scoff.ee.unsw.edu.au/information/information.htm](http://scoff.ee.unsw.edu.au/information/information.htm)

The major information headings are listed below.

Information for Current Students

USE OF EE&T FACILITIES

- Laboratory Regulations and Safety
- Evacuation Procedures
- OHS
- First Aid

ACADEMIC ISSUES

- The Learning experience
- Submission of Written Work
- Resubmission
- Late Submission
- Plagiarism and Academic Honesty
- UNSW Examination Rules
Equity and diversity: those students who have a disability that requires some adjustment in their teaching or learning environment are encouraged to discuss their study needs with the course convener prior to, or at the commencement of, their course, or with the Equity Officer (Disability) in the Equity and Diversity Unit (9385 4734 or www.equity.unsw.edu.au/disabil.html). Issues to be discussed may include access to materials, signers or note-takers, the provision of services and additional exam and assessment arrangements. Early notification is essential to enable any necessary adjustments to be made. Information on designing courses and course outlines that take into account the needs of students with disabilities can be found at: