ELEC4602
Microelectronics
Design and Technology

COURSE INTRODUCTION — session 2, 2014

Course Staff
Course convener: Torsten Lehmann, room EE-208, tlehmann@unsw.edu.au
Laboratory demonstrator: Tanvir Rahman

Consultations: Students are encouraged to use lectures and the open consultation hour to ask questions on course material, rather than by email; students may seek consultation with the course convener at other times by appointment.
Consultations: Tuesdays, 1pm–2pm, room EE-231A/EE-208

Course details
Credits: The course is a 6 UoC course; expected workload is 10–12 hours per week throughout the 13 week session.

Contact hours: The course consist of 2 hours of lectures per week, and 2 hours of laboratory sessions per week:
Lectures: Tuesdays, 12pm–1pm, room Quad-G026
          Wednesdays, 3pm–4pm, room Quad-G025
Lab sessions: Tuesdays, 4pm–6pm, room EE-214, or
              Thursdays, 6pm–6pm, room EE-214

Laboratory sessions start in week 3.

Course Information
Context and aims
Microelectronics or integrated electronics is the miniaturised electronic circuits that make up Integrated Circuits (ICs) such as microprocessors, Field-Programmable Gate Arrays, Flash-memories, operational amplifier, analogue-to-digital converters and many other functions. Most ICs today are implemented in various flavours of CMOS technology which is the focus of this course. The ability to use large number of components at relative low cost and the ability to match components accurately on-chip makes the design of integrated circuits and systems different from a similar design using discrete components. Microelectronics Design and Technology is
a broad based, introductory IC design course, which takes the student through all the necessary steps in order to complete (ready-to-manufacture) a basic mixed-signal front-end in a typical integrated system.

**Aims:** The course aims to make the student familiar with CMOS microelectronics technologies, and enable the student to do analysis and design of circuits implemented in these technologies.

**Relation to other courses**

The course is a fourth year professional elective offered to students following a BEE course at the University of New South Wales. The course gives the foundations for microelectronic circuit design and technology; as such, the course would normally be taken concurrently with thesis work in the microelectronic circuit design area.

**Pre-requisites:** The pre-requisites for the course is ELEC3106, Electronics. It is essential that the students are familiar with circuit theory and basic analogue and digital electronics as well as basic signal analysis as covered in the courses ELEC1111, ELEC2133, ELEC2141 and ELEC2132.

**Assumed knowledge:** It is further assumed that the students are familiar with SPICE-like circuit simulators, and have a good computer literacy.

**Following courses:** The course is a co-requisite for the post-graduate course ELEC9701, Mixed Signal Microelectronics Design, which is a core course in the microelectronics post-graduate program offered by the school.

**Learning outcomes**

After the successful completion of the course, the student will be able to

1. appreciate capabilities and limitations of current microelectronic (or IC) technologies,
2. use modern CAD design tools to design ICs,
3. create IC layouts,
4. understand and use circuit models of IC components,
5. analyse simple analogue and digital microelectronic circuits, and
6. design simple analogue, digital and mixed microelectronic circuits.

The course delivery methods and course content address a number of core UNSW graduate capabilities; these include:

1. The capability of being rigorous in analysis, critique and reflection, which is addressed by the laboratory work, design task and tutorial exercises.
2. The ability to apply knowledge and skills to solve problems, which is addressed by the lectures and design task.
3. The capability of effective communication, which are addressed by the reports.

4. The capability of independent, self-directed practice, which is addressed by the lectures and homework.

For more information about graduate capabilities, please refer to [http://teaching.unsw.edu.au/graduate-capabilities](http://teaching.unsw.edu.au/graduate-capabilities).

**Teaching strategies**

The course consists of the following elements: lectures, laboratory work, home work, self-guided tutorials and a design task:

**Lectures**

During the lectures technology capabilities and design issues are discussed and theoretical aspects of IC design and technology are presented. The lectures provide the students with a focus on the core material in the course, and a qualitative, alternative explanations. Numerous examples of analogue and digital integrated circuits are discussed in order to convey a qualitative understanding of circuit operations. The lectures aim to support students in analysing circuits and appreciate the capabilities of IC technologies. Importantly, the lectures also gives students the opportunity to seek clarification and ask questions in all course related areas. Students are expected to attend the lectures and prepare themselves for them.

**Laboratory work**

The laboratory work provides the student with hands-on design experience and exposure to state-of-the-art CAD tools. The laboratory work thus enables the students to use these tools for IC circuit design, analysis and lay-out. Students are required to attend the laboratory sessions and must come prepared for them; the laboratory sessions are short, so this is only possible way to complete the given tasks.

**Home work**

The lectures can only cover the course material to a certain depth; students must read the textbook and reflect on its content as preparation for the lectures to fully appreciate the course material. Home preparation for laboratory exercises provides the student with quantitative understanding of IC circuit analysis. The home work aim to provide in-depth quantitative and qualitative understanding of IC circuits and technologies. Note that no lecture notes will be handed out. The ability to read the recommended text book and identify critical parts with the aid of the lectures is regarded as an essential component of this course.

**Self-guided tutorials**

The self-guided tutorials provides the student with in-depth quantitative understanding of IC circuit analysis. The tutorials take the student through all critical course topics and aim to exercise the students IC circuit analysis skills. The students are strongly encouraged to complete all the tutorials; the problems may be discussed in the consultation hours.
A design task

The design task aims to draw together theoretical and practical design aspects in an open-ended realistic design problem. Students design an IC circuit meeting given specifications, use the CAD tools to verify the circuit operation and write a report documenting their design. The design task provide and test engineering creativity, open-ended problem solving skills, communication skills and general understanding of the course content. The design task involves design, theoretical analysis, computer simulations and layout of a microelectronic circuit is to be carried out in groups of one or two students. Students may use the CAD tools in room EEG16/EEG20 for this task. (Students are not to use the scheduled laboratory time for the design task).

Assessment

There are four components of the assessment in this course:

Laboratory work: 10% overall weight
Quizzes: 10% overall weight
Design task: 15% overall weight
Final examination: 65% overall weight

Assessment task due dates are given in the course schedule.

Laboratory work: The laboratory work is assessed in order to ensure that the students understand the material in this essential course component; thus, this assessment test that the student can use the CAD tools, understand circuit models and circuits, and can create IC layouts. Laboratory work must be documented in brief reports which are to be uploaded as .pdf files on the course Moodle site no later than Friday the due week. Late submissions carry a 50% penalty for the first week and will not be accepted beyond one week delay. Delays on medical grounds are accepted. Assessment is grade-only marks based on lab work and reports (a HD mark is given only for exceptional performance; a serious attempt at completing the problems is required for a PS mark).

Quizzes: There are two quizzes held during the lecture time through the semester. which are provided in order to give early feed-back on student performance. The quizzes test the students general understanding of the course material; assessment is a graded mark according to the correct fraction of the answers to the quiz questions.

Design task: The design task is assessed to test the students ability to design a simple integrated circuit, thus also demonstrating the students appreciation of the technology, and ability to use appropriate models and conduct suitable analysis to aid the design. A report on the design must be written which is to be uploaded as a .pdf file on the course Moodle site no later than Friday the due week. Late submissions carry a 50% penalty for the first week and will not be accepted beyond one week delay. Delays on medical grounds are accepted. Assessment is grade-only marks and are given on basis of the quality and innovativeness of the design (a HD mark is given only for exceptional performance; a serious attempt at completing the problems is required for a PS mark).
Final examination: The exam in this course is a standard closed-book 3 hours written examination; University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Assessment is a graded mark according to the correct fraction of the answers to the exam questions.

Course contents

| 1 | Topic: CMOS processing technology and components: lithography, implantation, etching, and other processing; MOS transistors, resistors, capacitors, inductors.  
Text: Baker ch. 7, web; Baker ch. 5. |
| 2 | Topic: IC layout: active, poly, contact, metal and other layers; design rules.  
Text: Baker ch. 3, 4, web. |
| 3 | Topic: Design, synthesis and verification tools. Layout editor, p-cells, cell libraries, P&R, VHDL compilers, process scaling, spice simulator, extraction, LVS.  
Text: Web.  
Tasks: Lab 1, layout with Cadence. |
| 4 | Topic: MOS models; device noise: NMOS and PMOS devices, operating regions, current equations, large/small signal models, analogue/digital models; noise.  
Text: Baker ch. 9, 10; Baker ch. 8.  
Tasks: Lab 1 continued. |
Text: Baker ch. 20, 21, 22.  
Tasks: Lab 2, circuit simulation with Cadence; Lab 1 report due. QUIZ 1. |
| 6 | Topic: Operational amplifiers: two-stage amplifiers, compensation, slew-rate, bandwidth, output stages.  
Tasks: Lab 2 continued. |
| 7 | Topic: Samplers; comparators: capacitive sampling, charge-injection; continuous and latched comparators.  
Text: Baker ch. 25; Baker ch. 27.  
Tasks: Lab 3, op-amp design; Lab 2 report due. |
| 8 | Topic: D/A and A/D converters: data converter fundamentals, current-steering, charge scaling DACs, flash and successive approximation ADCs.  
Text: Baker ch. 28, ch. 29.  
Tasks: Lab 3 continued. |
| 9 | Topic: CMOS inverters and logic: noise margins, voltage transfer characteristics, switching, gate delay, inverter sizing, fan-out, power dissipation.  
Text: Baker ch. 11.  
Tasks: Lab 4, combinational logic; Lab 3 report due. QUIZ 2. |
| Mid-semester Break |
| 10 | Topic: CMOS logic: static logic, complex gate synthesis, gate layout, gate sizing, special functions.  
Text: Baker ch. 12.  
Tasks: Lab 4 continued. |
| 11 | Topic: Sequential logic: transmission gates, multiplexers, latches and flip-flops, transistor sizing, set-up and hold times, dynamic registers.  
Tasks: Lab 5, sequential logic. Lab 4 report due. |
| 12 | Topic: Memory: ROM, SRAM and DRAM cell design, organisation and performance, sense amplifiers, floating-gate memory.  
Text: Baker ch. 16.  
Tasks: Lab 5 continued. |
| 13 | Tasks: No lab. Lab 5 report due. Design project due. |
Resources for Students

Textbooks

Prescribed textbook

The following textbook is prescribed for the course:


Students are expected to obtain a copy of this book as it provides the most coverage of the topics in the syllabus. Lecture notes will not be handed out.

Reference books

The following books are good additional resources for topics on analogue integrated circuit design, digital integrated circuit design and semiconductor device physics:


Books covering assumed knowledge

The following books cover material which is assumed knowledge for the course:


On-line resources
The course website will be used to disseminate course material. The course Moodle site will be used to host forums, upload reports, disseminate assessment results and for announcements. Key on-line course resources:
Resource: course website  http://subjects.ee.unsw.edu.au/elec4602
Moodle       http://moodle.telt.unsw.edu.au/
mosis website http://www.mosis.com
book website  http://www.cmosedu.com
library resources http://www.library.unsw.edu.au

CAD resources
Students will use the PCs in the CAD Laboratory (room 214) for all laboratory works. The CAD tools used in this course is the industry standard Cadence design suite which run under the Linux system on the dual boot PCs. For specific details on how to log on, see the course web page. Students can access the CAD tools after hours on the dual boot PCs in the School computer laboratory located in room EEG16/EEG20.

Other Matters
Academic Honesty and Plagiarism
Plagiarism is the unacknowledged use of other peoples work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a serious offence by the University and severe penalties may apply. For more information about plagiarism, please refer to https://my.unsw.edu.au/student/atoz/Plagiarism.html.

Student Responsibilities and Conduct
Students are expected to be familiar with and adhere to all UNSW policies, see https://my.unsw.edu.au/student/atoz/ABC.html: particular attention should be drawn to: workload, attendance, general conduct and behaviour, and work health and safety.

Keeping Informed: Announcements may be made during classes, via email (to student email addresses) or via online learning and teaching platforms like Moodle. From time to time, UNSW will send important announcements via these media without providing any paper copy. Students will be deemed to have received this information, and should take careful note of all announcements.

Special Consideration and Supplementary Examinations
Students must submit/attend all assessment components scheduled for the course. They should seek assistance early if they suffer illness or misadventure which affects their course progress. All applications for special consideration must be lodged online through myUNSW within 3 working days of the assessment, not to course or school staff. For more detail, consult https://my.unsw.edu.au/student/atoz/SpecialConsideration.html.
Continual Course Improvement

Students are advised that the course is under constant revision in order to improve the learning outcomes of its students. Please forward any feedback (positive or negative) on the course to the course convener, via the Course and Teaching Evaluation and Improvement Process, or to ELSOC. Previous feedback have led to web release of summary slides and changes to the assessment weighting.

Administrative Matters

On further issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the UNSW and School policies, see https://my.unsw.edu.au/student/atoz/ABC.html and http://www.engineering.unsw.edu.au/electrical-engineering.